

**CLAIMS**

What is claimed is:

1. A latch circuit for complementary dynamic logic, said latch circuit comprising:

2           a first logic gate having a first input and a second input, wherein said first  
3           input is connected to a first precharged internal node of said complementary  
4           dynamic logic, and said second input is connected to a first differential output of  
5           said complementary dynamic logic;

6           a second logic gate having a first input and a second input, wherein said first  
7           input is connected to a second precharged internal node of said complementary  
8           dynamic logic, and said second input is connected to a second differential output  
9           of said complementary dynamic logic;

10          a third logic gate having a first input connected to an output of said first  
11          logic gate to provide a first output for said latch circuit; and

12          a fourth logic gate having a first input connected to an output of said second  
13          logic gate to provide a second output for said latch circuit, wherein said second  
14          output is connected to a second input of said third logic gate, and said first output  
15          is connected to a second input of said fourth logic gate.

1       2.     The latch circuit of Claim 1, wherein said first and second outputs are differential  
2           outputs.

1       3.     The latch circuit of Claim 1, wherein inputs of said first and second logic gates are  
2           connected to transistors at the top of the stack of transistors within said first and second  
3           logic gates.

1        4. A latch circuit capable of ensuring race-free staging of signals for a dynamic logic  
2        circuit, said latch circuit comprising:

3                  a first NAND gate having a first input and a second input, wherein said first  
4        input is connected to a first precharged internal node of said complementary  
5        dynamic logic, and said second input is connected to a first differential output of  
6        said complementary dynamic logic;

7                  a second NAND gate having a first input and a second input, wherein said  
8        first input is connected to a second precharged internal node of said complementary  
9        dynamic logic, and said second input is connected to a second differential output  
10      of said complementary dynamic logic;

11                 a third NAND gate having a first input connected to an output of said first  
12      NAND gate to provide a first output for said latch circuit; and

13                 a fourth NAND gate having a first input connected to an output of said  
14      second NAND gate to provide a second output for said latch circuit, wherein said  
15      second output is connected to a second input of said third NAND gate, and said first  
16      output is connected to a second input of said fourth NAND gate.

1       5.     The latch circuit of Claim 1, wherein said first and second outputs are differential  
2           outputs.

1       6.     The latch circuit of Claim 1, wherein inputs of said first and second NAND gates  
2           are connected to transistors at the top of the stack of transistors within said first and second  
3           NAND gates.

1        7. A latch circuit capable of ensuring race-free staging of signals for a dynamic logic  
2        circuit, said latch circuit comprising:

3                  a first NOR gate having a first input and a second input, wherein said first  
4        input is connected to a first precharged internal node of said complementary  
5        dynamic logic, and said second input is connected to a first differential output of  
6        said complementary dynamic logic;

7                  a second NOR gate having a first input and a second input, wherein said first  
8        input is connected to a second precharged internal node of said complementary  
9        dynamic logic, and said second input is connected to a second differential output  
10      of said complementary dynamic logic;

11                 a third NOR gate having a first input connected to an output of said first  
12      NOR gate to provide a first output for said latch circuit; and

13                 a fourth NOR gate having a first input connected to an output of said second  
14      NOR gate to provide a second output for said latch circuit, wherein said second  
15      output is connected to a second input of said third NOR gate, and said first output  
16      is connected to a second input of said fourth NOR gate.

1       8.     The latch circuit of Claim 1, wherein said first and second outputs are differential  
2           outputs.

1       9.     The latch circuit of Claim 1, wherein inputs of said first and second NOR gates are  
2           connected to transistors at the top of the stack of transistors within said first and second  
3           NOR gates.